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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	6

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/761,122	Applicant(s) YAMAURA ET AL.
	Examiner David J. Huisman	Art Unit 2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *12-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: #5. Request for Reconsideration as received on 4/8/2004.

Election/Restrictions

3. Applicant's election with traverse of claims 1-11 in the reply filed on April 8, 2004, is acknowledged. The traversal is on the ground(s) that that "independent claim 1 is directed to a parallel processor comprising a global processor and a processor-element block comprising a plurality of processing elements, classified in class 712, and independent claim 12 is also directed to a parallel processor comprising a global processor and a processor-element block comprising a plurality of processing elements, classified in class 712." This is not found persuasive because there are additional details from each claim that have been left out of applicant's arguments. The restriction made by the previous examiner was drawn more to the additional details. In addition, the dependent claims of claim 12 differ from those of claim 1. Finally, even though both claims are classified in class 712, the class itself is divided into 90+ subclasses. Patents found in one subclass do not necessarily overlap with patents of another subclass. And, the examiner's search for the elected group of claims did not yield results which would also read on claims in the second group of claims (non-elected group).

The requirement is still deemed proper and is therefore made FINAL.

Specification

4. The abstract of the disclosure is objected to because of the following: Please remove the line break after the comma in line 6. Also, the first sentence (most specifically, the "control entirety" portion) is not understood by the examiner. Correction is required. See MPEP § 608.01(b).

5. A substitute specification in proper idiomatic English and in compliance with 37 CFR 1.52(a) and (b) is required. The substitute specification filed must be accompanied by a statement that it contains no new matter. Although this specification does not appear to be a direct translation, it is very difficult to read due to choice of wording and sentence structure. It would be beneficial to the public and to applicant to have a patent (if and when this application issues) which can be understood clearly. This would make it easier to use applicant's patent as prior art against similar applications in the future.

6. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

7. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

8. The disclosure is objected to because of the following informalities: On page 7, line 11, change "total 256" to --a total of 256--. On page 10, lines 21-22, change "an instructions" to either --an instruction-- or --instructions--. On page 17, line 12, replace "flab" with --flag--. On page 27, line 16, reference number 3a is not in Fig.1. On page 30, line 15, reference number 31b

is not in Fig.2. On page 30, line 22, replace "resisters" with --registers--. Replace all occurrences of "exmaple" with --example-- (such as the instance on page 44, line 22). Replace all occurrences of "copmarison" (and its variations) with --comparison-- (and its variations). On page 45, line 2, replace "compare" with --compared--. The phrase "valid/invalid of execution of operation" on page 75, line 11 is not understood by the examiner and should therefore be reworded. Replace all occurrences of "memroy" with --memory--.

Appropriate correction is required.

Drawings

9. The drawings are objected to because of the following: In Fig.10 and Fig.15, all of the 131d (???) reference numbers should be repositioned so that they can be clearly read (currently, they are overlapping bus 137). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

10. Claims 4 and 9 are objected to because of the following informalities: In claim 4, the examiner believes that "thus-" can be deleted. Appropriate correction is required.

Claim Rejections - 35 USC § 112

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claim 1 recites the limitation "the processor" in line 3 of the claim. There is insufficient antecedent basis for this limitation in the claim because both a "global processor" and a "parallel processor" had been mentioned previously.

13. Claims 2-11 recite the limitation "The processor as claimed in..." in the first line of each claim. There is insufficient antecedent basis for this limitation in the claim because both a "global processor" and a "parallel processor" had been mentioned previously.

14. The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors. Consequently, the examiner has interpreted the claims in the most reasonable fashion possible.

Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

16. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Applicant's Admitted Prior Art (herein referred to as AAPA).

17. Referring to claim 1, AAPA has taught a parallel processor comprising:

a) a global processor interpreting a program and controlling the entirety of the processor. See page 3, lines 7-10, of applicant's background.

b) processor-element block comprising a plurality of processor elements each comprising a register file and an operation array for processing a plurality of sets of data. See page 3, lines 3-6, of applicant's background.

c) wherein said global processor outputs a control signal to said plurality of processor elements, and, thereby, sets processor-element numbers corresponding to said plurality of processor elements as input values of the operation arrays, respectively. See page 11, lines 2-17, and note that processor element numbers are set and used in testing the processor element. More specifically, if the processor number is used in testing, then the number must be an input of circuitry which processes data. This teaching is prior art because applicant refers to this as being "related art" on page 11, line 9, and applicant follows with saying "However, in the above mentioned methods according to the present invention..." on page 11, line 18. Clearly, applicant is comparing the prior art with the present invention.

18. Claims 1 and 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaneko et al., U.S. Patent No. 5,430,885 (herein referred to as Kaneko).

19. Referring to claim 1, Kaneko has taught a parallel processor comprising:

a) a global processor interpreting a program and controlling the entirety of the processor. See Fig.1, component 401.

b) processor-element block comprising a plurality of processor elements each comprising a register file and an operation array for processing a plurality of sets of data. See Fig. 1, components 411, 412, 413, etc. Also, see column 1, lines 19-25. Note that coprocessors carry out tasks and therefore, would inherently contain a register file (for storing data) and an operation array for execution purposes.

c) wherein said global processor outputs a control signal to said plurality of processor elements, and, thereby, sets processor-element numbers corresponding to said plurality of processor elements as input values of the operation arrays, respectively. See column 3, lines 33-47, and note that each processor element (coprocessor) has a register (Fig.6, components 701 and 702, for instance) for storing a processing element number assigned to it by the host processor. And, from Fig.6, this processor number is inputted into at least a portion of the operation array (logic which processes data).

20. Referring to claim 7, Kaneko has taught a processor as described in claim 1. Kaneko has further taught that each processor element comprises a plurality of flag bits for controlling, according to a state of the data, as to whether or not the operation processing is to be executed, according to whether or not a condition is satisfied, and, renders AND/OR operation on a specific bit of said flag bits. Looking at Fig.8A, each processing element comprises (or is associated with) two flag bits; an X-coordinate flag bit 502 and a Y-coordinate flag bit 503. The global processor will specify X and Y vectors and if both the X and Y coordinate flag bits for each processing element are 1, then that processor will be enabled for execution purposes. So, for instance, looking at Fig.8A, processor 304 is enabled because its X-bit is set to 1 and its Y-bit is set to 1. However, the processing element directly left of element 304 is disabled because its

X-bit is set to 0 and its Y-bit is set to 1. Therefore, it can be seen that an AND operation must be performed on the X-bit. That is, the X-bit AND the Y-bit must be equal to 1 (XY = 1) for enablement to occur. See Fig.13 for an enablement flowchart.

21. Referring to claim 8, Kaneko has taught a processor as described in claim 7. Kaneko has further taught that specifying of said flag bits is rendered by specifying the range from the first specific processor element through the second specific processor element through specifying the immediate values by using the operands. Again, see Fig.8A, and note that immediate values 01100 (502) and 0110 (503), which are specified by the global processor, correspond to a range of processors that will be enables. These immediate values contain the flag bits which specify the range of elements which will be enabled.

22. Referring to claim 9, Kaneko has taught a processor as described in claim 7. Kaneko has further taught that specifying of said flag bits is rendered through specifying bits such as to specify processor elements matching processor-element numbers expressed in binary notation and specifying processor elements by masking arbitrary bits of the thus-specified bits through specifying the immediate values by using the operands. It should be realized that the flag bits merely play a part in determining which processing element(s) will be enabled. Furthermore, see Fig.6 and note that a comparison occurs between the number assigned to the processor (mask) and the number specified by the global processor. This assigned number is a mask because it is used to determine the value of bit locations in another value (the value specified by the global processor), which is the purpose of a mask. More specifically, the mask is used in a comparison. If the values are equal, then the system knows that the corresponding coprocessor will be enabled. And, these numbers are integers, which are in turn immediate values. Finally, even the

output of AND gate 709 in Fig.6 is a flag bit in that through specifying bits which either match or do not match the processor number, this flag is produced which either enables or disables the coprocessor from receiving input through input unit 710 for execution.

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaneko, as applied above.

25. Referring to claim 2, Kaneko has taught a processor as described in claim 1. Kaneko has further taught that data is transferred from the global processor to the coprocessors. See the abstract and column 2, lines 3-12. Kaneko has not explicitly taught that the transferred data came from the register file of the global processor. However, Official Notice is taken that register files and register file transfers between multiple processors are well known and accepted in the art. Data is generally stored in memories such as register files, data caches, main memory, hard disk, etc. However, register files are accessed the quickest, and therefore, would result in the fastest data transfer. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to transfer data from the register file of Kaneko's global processor to the processing elements.

26. Referring to claim 3, Kaneko has taught a processor as described in claim 2. Kaneko has further taught that the data transfer is rendered through specifying a range from a first specific processor element through a second specific processor element by specifying immediate values by using operands. See Fig.12B and column 10, lines 14-29, and note that the global processor specifies an entire range of coprocessors by issuing a designation number in the form of P(a, b, c, d). Clearly, this will be an operand of some form of transmit (or communicate) instruction. Also, a, b, c, and d are integers, which are in turn, immediate values.

27. Referring to claim 4, Kaneko has taught a processor as described in claim 2. Kaneko has further taught that the data transfer is rendered through specifying bits such as to specify processor elements matching processor-element numbers expressed in binary notation and specifying processor elements by masking arbitrary bits of the thus-specified bits, through specifying the immediate values by using the operands. See Fig.6 and note that a comparison occurs between the number assigned to the processor (mask) and the number specified by the global processor. This assigned number is a mask because it is used to determine the value of bit locations in another value (the value specified by the global processor), which is the purpose of a mask. More specifically, the mask is used in a comparison. If the values are equal, then the system knows that the corresponding coprocessor will be used in communication. And, these numbers are integers, which are in turn immediate values.

28. Claims 5-6 and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaneko, as applied above, in view of Hennessy and Patterson, "Computer Architecture - A Quantitative Approach, 2nd Edition," 1996 (herein referred to as Hennessy).

29. Referring to claim 5, Kaneko has taught a processor as described in claim 2. Kaneko has not taught that the data transfer is rendered through specifying by a pointer using a general-purpose register of said global processor. However, Hennessy has taught specifying a pointer using a general-purpose register on page 75 (see the indirect addressing mode). This mode is also used when loading (transferring) data to a register. See page 100. By implementing this indirect mode, Kaneko's system would not be restricted to merely transferring data from register file to register file. Instead, by using pointers, data can be transferred from main memory, which would be beneficial just in case a lot of data needs to be transferred and there aren't enough registers to store the data. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kaneko in view of Hennessy such that a data transfer is rendered by specifying a pointer using a register.

30. Referring to claim 6, Kaneko in view of Hennessy has taught a processor as described in claim 5. Kaneko has not taught that the specifying by a pointer comprises incrementing of data in said general-purpose register after the specifying. However, Hennessy has taught incrementing the contents of the register after the specifying. See the autoincrement mode on page 75. As explained in Fig.2.5 of Hennessy, the autoincrement mode is useful for transferring a block of data, for instance, which may be governed by a loop. By implementing this mode, Kaneko's system would not be restricted to merely transferring data from register file to register file. Instead, by using pointers, data can be transferred from main memory, which would be beneficial just in case a lot of data needs to be transferred and there aren't enough registers to store the data. In addition, if a block of data needs to be transferred, a second instruction would not be needed to increment the register data each time because the single instruction does it

automatically. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kaneko in view of Hennessy such that after specifying a pointer using a register, incrementing the contents of the register.

31. Referring to claim 10, Kaneko has taught a processor as described in claim 7. Kaneko has not explicitly taught that specifying of said flag bits is rendered through specifying by a pointer using a general-purpose register of said global processor. However, Hennessy has taught specifying data via specifying a pointer using a general-purpose register on page 75 (see the indirect addressing mode). By implementing this indirect mode, Kaneko's system would not be restricted to using immediate values to specify flag bits. Instead, by using pointers, the flag bits may be produced from main memory, thereby offering greater flexibility to the programmer. This may be beneficial because immediate values are not dependent on past operation. On the other hand, the programmer may want to use a processing-element configuration based on some data produced during previous execution. With indirect addressing, this data may be used to determine the appropriate flag bits, which specify the configuration of elements (which processing elements should be enabled), and the bits can be stored in main memory for future use. This flexibility is not available with immediate values only. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kaneko in view of Hennessy such that flag bits are specified via specifying a pointer using a register.

32. Referring to claim 11, Kaneko has taught a processor as described in claim 10. Kaneko has not explicitly taught that the specifying by a pointer comprises incrementing of data in said general-purpose register after the specifying. However, Hennessy has taught incrementing the contents of the register after the specifying. See the autoincrement mode on page 75. As

explained in Fig.2.5 of Hennessy, the autoincrement mode is useful for accessing linear data within a loop. By implementing this mode, Kaneko's system would be able to quickly achieve different preset processing-element configurations (for instance, multiple combinations of flag bits may be stored in main memory). Instead of having two instructions to first access flag bits from one address and then updating the address itself, only one instruction is needed to both access the flag bits and update the address so a next address can be read from. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kaneko in view of Hennessy such that after specifying a pointer using a register, incrementing the contents of the register.

Conclusion

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Barry et al., U.S. Patent No. 6,581,152, has taught methods and apparatus for instruction addressing in indirect VLIW processors. More specifically, Barry has disclosed assigning each processing element a unique ID and inputting this ID into computation circuitry for a processing-element relative addressing mode.

Li et al., U.S. Patent No. 4,783,738, has taught adaptive instruction processing by array processor having processor identification and data dependent status registers in each processing element.

Spielman et al., U.S. patent No. 5,600,811, has taught a vector move instruction in a vector data processing system and method therefor. In addition, a single flag bit associated with each processing element has been disclosed which dictates whether the element executes or essentially sits idle.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (703) 305-7811. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
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June 11, 2004

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